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| EXAMINER | |
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| KHAN, USMAN A | |
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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/664,918 | OGURA ET AL. | |
| | Examiner | Art Unit | |
| | Usman Khan | 2622 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *08 December 2005 and 28 March 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3 and 5-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3 and 5-13* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 September 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

***Response to Arguments***

Applicant's arguments filed on 03/28/2007 with respect to claims 1 – 3 and 5 - 13 have been considered but are not persuasive.

Applicant's arguments filed on 03/28/2007 with respect to claims 1 – 3 and 5 - 13 have been considered but are moot in view of the new ground(s) of rejection.

Regarding objection to drawings provided in the previous office action for failing to label prior art in figures 7A, 7B, and 8. Applicant has amended the drawings of the invention to overcome the objection to the drawings.

Regarding objection to claims 2, 3, 5, 6, 7, 8 provided in the previous office action. Applicant has amended claims 2, 3, 5, 6, and 7 to overcome the objections to these claims. Also, the examiner has withdrawn the objection to claim 8 in response to the applicant's arguments.

Examiner would like to thank the applicants for pointing out some mistakes in the "Office Action Summary" sheet. Accordingly in this "Office Action Summary" sheet the communication date of "08 December 2006" has been changed to "08 December 2005". Also, the pending claims and rejected claim numbering has been corrected from "1-8" to "1-3 and 5-13". This correction does not affect the rejections/objections made in the previous office actions and were mistakes only affecting the "Office Action Summary" sheet.

Please refer to the following office action, which clearly sets forth the reasons for non-persuasiveness.

In response to applicant's argument that in claims 1:

Regarding **claims 1**, Applicant argues that the claim distinguish over Suzuki in further view of Applicants admitted prior art by that pad electrode 116B is for pixel 130 of pixel part 110B, but that such provides signals indicating the degree of shading, for shading correction, and not output signals for generating image data; instead, pad electrode 116A (not 116B) outputs signals indicating image data. However it is clear from paragraphs 0060 – 0064 that the output amps 115A and 115B are separate and an average output signal of the pixels 130 is output through 116b for generating image data. Also, the output signal from the available pixel part 110B (i.e. leading to 116B) can be quickly read externally, such as by an analog signal processing circuit 227.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1 – 2, 5 – 8, and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US PgPub 2002/0025164) in further view of Applicants admitted prior art.

Regarding **claim 1,** Suzuki teaches a solid state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 items 110A and 110B); a pad for outputting an output of the amplifier to an outside of the chip (figure 1, items 110B, 115B, and pad 116B; also paragraphs 0060 - 0064, the shading pixel signals from 110B are sent through the amplifier 115B and output to pad electrode 116B; this pad electrode is located near the right vertical side of the pixel array; also the output amps 115A and 115B are separate and an average output signal of the pixels 130 is output through 116b for generating image data. Also, the output signal from the available pixel part 110B [i.e. leading to 116B] can be quickly read externally, such as by an analog signal processing circuit 227). An amplifier for amplifying the signal charge read from the pixel region and outputting the video signal (figure 1, items 110B and amplifier 115B; also paragraphs 0060 - 0064, the shading pixel signals from 110B are sent through the amplifier 115B).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. the amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower

driving frequency than that of the first shift register. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. the amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad 116B of Suzuki will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located). The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of

addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claim 2**, as mentioned above in the discussion of claim 1, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, Suzuki teaches that the pixel region, pixels having an active element are two-dimensionally arranged (figure 1 items 110A and 110B).

Regarding **claim 5**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, Suzuki teaches that the pixel region is formed into a rectangle, and the first shift register is arranged closer to a long side of the pixel region (figure 1).

Regarding **claim 6**, as mentioned above in the discussion of claim 5, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, applicant admitted prior art teaches that the pixel region is sandwiched by shift registers (figure 8, shift register 202 and 205 in essence sandwich the region close to where they form a right angle to each other).

Regarding **claim 7**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. Additionally, applicant admitted prior art teaches that the first shift register is a horizontal shift register (figure 8, item 205), and the second shift register is a vertical shift register (figure 8, item 202).

Regarding **claim 8**, Suzuki teaches a camera with a solid state image pick-up device formed on a chip (paragraph 0001 *et seq.*), comprising: a pixel region (figure 1 items 110A and 110B); a pad for outputting an output of the amplifier to an outside of the chip (figure 1, items 110B, 115B, and pad 116B; also paragraphs 0060 - 0064, the shading pixel signals from 110B are sent through the amplifier 115B and output to pad electrode 116B; this pad electrode is located near the right vertical side of the pixel array; also the output amps 115A and 115B are separate and an average output signal of the pixels 130 is output through 116b for generating image data. Also, the output signal from the available pixel part 110B [i.e. leading to 116B] can be quickly read externally, such as by an analog signal processing circuit 227). An amplifier for amplifying the signal charge read from the pixel region and outputting the video signal (figure 1, items 110B and amplifier 115B; also paragraphs 0060 - 0064, the shading pixel signals from 110B are sent through the amplifier 115B). A lens for forming an optical image of a subject (figure, 19); and a signal-processing unit for processing a signal from the solid-state image pick-up device (figure 16, item 221 controlling the

processing of the various components in the camera which in turn controls the processing of the signals).

However, Suzuki fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. The second shift register having a lower driving frequency than that of the first shift register.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register (figure 8 item 207). The pad being arranged only along a side portion of the chip different from the side portion along which

the first shift register is arranged (when applicants admitted prior art is combined with Suzuki invention the pad 116B of Suzuki will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located). The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claim 11**, as mentioned above in the discussion of claim 1 Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claims. Additionally, applicant admitted prior art teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Suzuki to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior

art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Claim 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki (US PgPub 2002/0025164) in further view of applicants admitted prior art in further view of Itano et al. (US PgPub 2002/0051071).

Regarding **claim 3**, as mentioned above in the discussion of claim 2, Suzuki in further view of applicant admitted prior art teaches all of the limitations of the parent claim. However, Suzuki in further view of applicant admitted prior art fail to disclose that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor. Itano et al., on the other hand teaches that the active element comprises at least one selected from the group consisting of a transfer MOS transistor, a reset MOS transistor, a source follower input MOS transistor, and a selection MOS transistor.

More specifically, Itano et al. teaches the active element comprises at least one selected from the group consisting of a transfer MOS transistor (figure 1 item 105, and paragraph 0006), a reset MOS transistor (figure 1 items 110a and 110b, and paragraph 0006), a source follower input MOS transistor (figure 1 item 107, and paragraphs 0006, 0048, 0051), and a selection MOS transistor (paragraph 0051).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate the teachings of Itano et al. with the teachings of Suzuki in further view of applicant admitted prior art for reduction of size and in turn cost as taught in paragraph 0021 of Itano et al.

Claims 9, 10, 12, and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kozuka et al. (US patent No. 6,118,115) in further view of Applicants admitted prior art.

Regarding **claim 9,** Kozuka et al. teaches a solid-state image pick-up device formed on a chip (column 5 liens 32 *et seq.*), comprising: a pixel region (figures 3 - 8 item 202 and column 5 liens 32 *et seq.*); An amplifier for amplifying the signal charge read from the pixel region (figure 3 and 8 items 13 - 14 leading to item 15). A pad for supplying a voltage to the amplifier (figure 7 item 100').

However, Kozuka et al. fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal. The second shift register having a lower driving frequency than that of the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register;

wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal. The second shift register having a lower driving frequency than that of the first shift register. The pad being only arranged along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Kozuka et al. invention the pad 100' of Kozuka et al. will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal (figure 8 item 207). The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Kozuka et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up

element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claim 10**, Kozuka et al. teaches a solid-state image pick-up device formed on a chip (column 5 liens 32 *et seq.*), comprising: a pixel region (figures 3 - 8 item 202 and column 5 liens 32 *et seq.*); An amplifier for amplifying the signal charge read from the pixel region (figure 3 and 8 items 13 - 14 leading to item 15). A pad for supplying a predetermined voltage or a ground voltage to an active element included in a pixel in the pixel region (figure 7 item 100).

However, Kozuka et al. fails to disclose that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal. The second shift register having a lower driving frequency than that of the first shift register. The pad being arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged. Applicants admitted prior art, on the other hand teaches that a first shift register for reading a signal charge from the pixel region, a second shift register; wherein the first and second shift registers are arranged along respectively different side portions of the chip. The amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal. The second shift register having a lower driving frequency than that of the first shift register. The pad being

arranged only along a side portion of the chip different from the side portion along which the first shift register is arranged (when applicants admitted prior art is combined with Kozuka et al. invention the pad 100 of Kozuka et al. will be arranged along a side portion of the chip different from the side portion along which the horizontal (i.e. first) shift register is located.

More specifically, admitted prior art teaches a first shift register for reading a signal charge from the pixel region (figure 8, item 205), a second shift register (figure 8, item 202); wherein the first and second shift registers are arranged along respectively different side portions of the chip (figure 8). the amplifier for amplifying the signal charge read from the pixel region by the first shift register outputting video signal (figure 8 item 207). The second shift register having a lower driving frequency than that of the first shift register (paragraph 0014).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Kozuka et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

Regarding **claims 12 - 13**, as mentioned above in the discussion of claims 9 and 10 respectively, Kozuka et al. in further view of applicant admitted prior art teaches all of

the limitations of the parent claims. Additionally, applicant admitted prior art teaches that the side portions along which the first and second shift registers are arranged are adjacent to each other (figure 8).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to applicants admitted prior art of horizontal and vertical shift registers with the teachings of Kozuka et al. to have a simple and reliable way of addressing and reading out pixels. Also, in paragraph 0007 applicants admitted prior art teaches that the use of the prior art will produce a tightly sealed image pick-up element in turn this will produce better quality images without external distortion and a higher quality image pick-up element protected from external impurities.

***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR1.136(a) will be calculated from the mailing date of the

advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Usman Khan whose telephone number is (571) 270-1131. The examiner can normally be reached on Mon-Thru 6:45-4:15; Fri 6:45-3:15 or Alt. Fri off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Usman Khan
05/16/2007
Patent Examiner
Art Unit 2622

DAVID OMETZ
SUPERVISORY PATENT EXAMINER